IN THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) A signal transmission circuit for transmitting a digital signal from a first circuit block to a second circuit block via a signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period,

the first circuit block comprising a transmitting circuit including:

a transmitting capacitor;

an input switch for ~~setting~~ supplying an input digital signal to the transmitting capacitor for each preparation period so as to set a voltage in accordance with a logic level of said ~~a supplied~~ input digital signal in the transmitting capacitor at each preparation period; and

a transmitting switch for ~~generating~~ connecting the transmitting capacitor to the signal line for each transmission period so as to generate a small voltage change in the signal line at each transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period,

the second circuit block comprising a receiving circuit including:

an inverter connected to the signal line;

an equalizing switch for short-circuiting ~~the~~ an input terminal and ~~the~~ an output terminal of the inverter so as to set a voltage of the signal line to a predetermined voltage at each preparation period; and

a latch for supplying an output digital signal obtained by performing logic amplification of a voltage of the output terminal of the inverter at each transmission period.

2. (Currently amended) A signal transmission circuit for transmitting a digital signal from a first circuit block to a second circuit block via a signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period,

the first circuit block comprising a transmitting circuit including:

a transmitting capacitor;

an input switch for ~~setting~~ supplying an input digital signal to the transmitting capacitor for each preparation period so as to set a voltage in accordance with a logic level of said ~~a supplied~~ input digital signal in the transmitting capacitor at each preparation period; and

a transmitting switch for ~~generating~~ connecting the transmitting capacitor to the signal line for each transmission period so as to generate a small voltage change in the signal line at each transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period,

the second circuit block comprising a receiving circuit including:

an inverter connected to the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch for short-circuiting the input terminal and the output terminal of the inverter so as to set a voltage of the receiving capacitor to a predetermined voltage at each preparation period; and

a latch for supplying an output digital signal obtained by performing logic amplification of a voltage of the output terminal of the inverter at each transmission period.

3. (Currently amended) A signal transmission circuit for transmitting a digital signal from a first circuit block to a second circuit block via a signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period,

the first circuit block comprising a transmitting circuit including:

a transmitting capacitor;

an input switch for ~~setting~~ supplying an input digital signal to the transmitting capacitor for each preparation period so as to set a voltage in accordance with a logic level of said ~~a supplied~~ input digital signal in the transmitting capacitor at each preparation period; and

a transmitting switch for ~~generating~~ connecting the transmitting capacitor to the signal line for each transmission period so as to generate a small voltage change in the signal line at each transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period,

the second circuit block comprising a receiving circuit including:

an inverter connected to the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch for short-circuiting the input terminal and the output terminal of the inverter so as to set a voltage of the signal line to a predetermined voltage at each preparation period; and

a latch for holding an output digital signal obtained during a preceding transmission period at each preparation period.

4. (Currently amended) A signal transmission circuit for transmitting a digital signal from a first circuit block to a second circuit block via a signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period,

the first circuit block comprising a transmitting circuit including:

a transmitting capacitor;

an input switch for ~~setting~~ supplying an input digital signal to the transmitting capacitor for each preparation period so as to set a voltage in accordance with a logic level of said ~~a supplied~~ input digital signal in the transmitting capacitor at each preparation period; and

a transmitting switch for ~~generating~~ connecting the transmitting capacitor to the signal line for each transmission period so as to generate a small voltage change in the signal line at each transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period,

the second circuit block comprising a receiving circuit including:

an inverter connected to the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch for short-circuiting the input terminal and the output terminal of the inverter so as to set a voltage of the signal line to a predetermined voltage at each preparation period; and

a latch for supplying an output digital signal obtained by performing logic amplification of a voltage of the output terminal of the inverter for each transmission period and holding the output digital signal obtained during a preceding transmission period for each preparation period.

5. (Currently amended) A signal transmission circuit for transmitting a digital signal from a first circuit block to a second circuit block via a signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period,

the first circuit block comprising a transmitting circuit including:

a transmitting capacitor;

an input switch designed to be on to supply an ~~a supplied~~ input digital signal to the transmitting capacitor for each preparation period so as to set a voltage in accordance with a logic level of the input digital signal in the transmitting capacitor at each preparation period, and to be off for each transmission period; and

a transmitting switch designed to be on to connect the transmitting capacitor to the signal line for each transmission period so as to generate a small voltage change in the signal line at each transmission period, the voltage change being in accordance with a

voltage of the transmitting capacitor that is set during a preceding preparation period, and to be off for each preparation period,

the second circuit block comprising a receiving circuit including:

an inverter connected to the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch designed to be on to short-circuit the input terminal and the output terminal of the inverter for each preparation period so as to set each voltage of the signal line and the input terminal and the output terminal of the inverter to a predetermined equalized voltage at each preparation period, and to be off to allow an operation of the inverter for amplifying a small voltage change in the signal line for each transmission period so as to charge and discharge the receiving capacitor; and

a latch for supplying an output digital signal obtained by performing logic amplification of a voltage of the output terminal of the inverter for each transmission period and holding the output digital signal obtained during a preceding transmission period for each preparation period.

6. (Currently amended) The signal transmission circuit according to claim 5, further comprising a cut-off switch for separating the inverter from a power line after the setting of the equalized voltage is completed at each preparation period.

7. (Currently amended) The signal transmission circuit according to claim 5, further comprising a cut-off switch for separating the inverter from a power line after a voltage of the output terminal of the inverter is established at each transmission period.

8. (Currently amended) A signal transmission circuit for transmitting a digital signal from ~~either one~~ a circuit block of a first circuit block group to a second circuit block via a common signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period,

each circuit block of the first circuit block group comprising a transmitting circuit including:

a transmitting capacitor;

an input switch designed to be on to supply an ~~a supplied~~ input digital signal to the transmitting capacitor for each preparation period so as to set a voltage in accordance with a logic level of the input digital signal in the transmitting capacitor at preparation period, and to be off for each transmission period;

a transmitting switch designed to be on to connect the transmitting capacitor to the signal line for each transmission period so as to generate a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period, and to be off for each preparation period; and

a logic circuit for changing each state of the input switch and the transmitting switch in response to the clock signal when a corresponding selection signal is activated, and for fixing each state of the input switch and the transmitting switch when the selection signal is non-activated,

the second circuit block comprising a receiving circuit including:

an inverter connected to the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch designed to be on to short-circuit the input terminal and the output terminal of the inverter for each preparation period so as to set each voltage of the signal line and the input terminal and the output terminal of the inverter to a predetermined equalized voltage at each preparation period, and to be off to allow an operation of the inverter for amplifying a small voltage change in the signal line for each transmission period so as to charge and discharge the receiving capacitor; and

a latch for supplying an output digital signal obtained by performing logic amplification of a voltage of the output terminal of the inverter for each transmission period and holding the output digital signal obtained during a preceding transmission period for each preparation period.

9. (Currently amended) A signal transmission circuit for transmitting a digital signal from a first circuit block to ~~either one~~ a circuit block of a second circuit block group via a common signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period,

the first circuit block comprising a transmitting circuit including:

a transmitting capacitor;

an input switch designed to be on to supply an ~~a supplied~~ input digital signal to the transmitting capacitor for each preparation period so as to set a voltage in accordance with a logic level of the input digital signal in the transmitting capacitor at preparation period, and to be off for each transmission period; and

a transmitting switch designed to be on to connect the transmitting capacitor to the signal line for each transmission period so as to generate a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period, and to be off for each preparation period;

each circuit block of the second circuit block group comprising a receiving circuit including:

an inverter connected to the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch designed to be on to short-circuit the input terminal and the output terminal of the inverter for each preparation period so as to set each voltage of the signal line and the input terminal and the output terminal of the inverter to a predetermined equalized voltage at each preparation period, and to be off to allow an operation of the inverter for amplifying a small voltage change in the signal line for each transmission period so as to charge and discharge the receiving capacitor;

a latch for supplying an output digital signal obtained by performing logic amplification of a voltage of the output terminal of the inverter for each transmission period and holding the output digital signal obtained during a preceding transmission period for each preparation period; and

a logic circuit for changing a state of the equalizing switch in response to the clock signal when a corresponding selection signal is activated, and for fixing the equalizing switch to be off when the selection signal is non-activated.

10. (Currently amended) A signal transmission circuit for transmitting a logic operation result from a first circuit block group to a second circuit block via a common signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period, the logic operation result being based on a digital signal supplied to ~~each~~ circuit blocks of the first circuit block group,

each circuit block of the first circuit block group comprising a transmitting circuit including:

a transmitting capacitor;

an input switch designed to be on to supply a predetermined logic voltage to the transmitting capacitor for each preparation period so as to set the logic voltage in the transmitting capacitor at preparation period, and to be off for each transmission period;

a transmitting switch designed to be on to connect the transmitting capacitor to the signal line for each transmission period so as to generate a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period, and to be off for each preparation period; and

a logic circuit for changing each state of the input switch and the transmitting switch in response to the clock signal when a corresponding input digital signal is activated, and for fixing each state of the input switch and the transmitting switch when the input digital signal is non-activated,

the second circuit block comprising a receiving circuit including:

an inverter connected to the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch designed to be on to short-circuit the input terminal and the output terminal of the inverter for each preparation period so as to set each voltage of the signal line and the input terminal and the output terminal of the inverter to a predetermined equalized voltage at each preparation period, and to be off to allow an operation of the inverter for amplifying a small voltage change in the signal line for each transmission period so as to charge and discharge the receiving capacitor; and

a latch for amplifying a voltage of the output terminal of the inverter by performing logical determination with a logic threshold voltage different from the equalized voltage so that an output digital signal indicating the logic operation result is obtained for each transmission period and holding the output digital signal obtained during a preceding transmission period for each preparation period.

11-19. (Cancelled)